CND 221
ADVANCED FULL CUSTOM VLSI DESIGN
2023

Course Description

The main objective of this course is to introduce the students to modern advanced full custom VLSI digital integrated circuits. The student will be introduced to the implementation strategies in digital IC design, dealing with timing issues. In addition, the interconnect modeling and spice wire model will be demystified. The students get hands-on experience in using modern industrial CAD tools.

Contact Hours

Credit Hours	Lecture Hours	Lab Hours	Student work	Total
6	24 (1.25x2)/week	21 (3x1)/week	48	93

Prerequisites

Introduction to Silicon Process and VLSI

Learning Outcomes

After successful completion of this course, the student will be able to:

1. Practice, Design, and understand advanced CMOS digital integrated circuits through a hands-on design process including:
    - Practicing and understanding VLSI design flows starting from circuit design, pre-layout simulation, layout creation, Design rule check (DRC), layout vs schematic (LVS), parasitic extraction, full annotation, testing and verification, and post layout simulation.
    - Understanding the different design flows such as non-programmable (e.g., ASIC) and programmable design flows.
    - Practice and understand the differences among full-custom, semi-custom, cell-based, and array-based design flows.
2. Practice, understand, and design module level building blocks including arithmetic building blocks and memory structures.
3. Practice, Analyze, understand, and tackle system level challenges including timing issues, interconnect parasitic effects, testing and verification, power distribution, I/Os, and clock distributions.

Course Materials

Textbook:

- Rabaey, Jan, Anantha Chandrakasan, and Bora Nikolic. Digital Integrated Circuits: A Design Perspective. 2nd ed. Prentice Hall.

References:

- Weste, Neil, Harris, David. CMOS VLSI Design: A Circuits and Systems Perspective 4th Ed. Pearson.
- Johnson, Howard, Graham, Martin. High Speed Digital Design: A Handbook of Black Magic. Pearson.
- Material is also derived from the IEEE Journals, Transactions, and flagship Conference proceedings.

Tools Use in Lab:

- Siemens EDA flow: Tanner EDA (S-Edit (Schematic Editor), L-Edit (Layout Editor), W-Edit (Waveform Editor) and Calibre.

Course Project: By the end of this course the students are required to deliver a complete project (chosen from variety of proposals) assigned by the industry experts and university professors instructors.

Course Topics and Schedule

Week	Lecture	Readings	Lab
Revision on Combinational and Sequential Logic			

1	• Revision on Combinational and Sequential Logic.
	• C^2MOS: A clock skew insensitive approach.
	• Alternative Register Styles
	  ○ Pulse Registers
	  ○ Sense-Amplifier Based Registers
	• Pipelining: An approach to optimize sequential circuits
	  ○ Latch- vs. Register-Based Pipelines
	  ○ NORA-CMOS—A Logic Style for Pipelined Structures
	• Non-Bistable Sequential Circuits
	  ○ The Schmitt Trigger
	  ○ Monostable Sequential Circuits
		Rabaey: Ch7. 7.3.2, 7.4 Ch7: 7.5, 7.6	**LAB01: Implementing Pulse Registers**

	○ Astable Circuits		
<u>VLSI Design Flows (Learning Outcome 1)</u>			
2	Overview and Introduction to advanced full custom VLSI design Flow: • Introduction to VLSI Design Flow (ASIC flow, Behavioral and structural design, (From Specification to layout and Chip Design). • From Custom to Semi-custom and Structured Array Design Approaches. • Custom Circuit Design Example: "Differential input output CMOS (DINO-CMOS)".	Rabaey: 8.1, 8.2	**LAB02: Pipelined Data Path with C2MOS Latches (NORA-CMOS).**
3	**<u>Advanced full custom VLSI design Flow</u>** • Cell-Based Design Methodology ○ Standard Cell ○ Compiled Cells ○ Macrocells, Megacells and Intellectual Property ○ Semi-Custom Design Flow • Array-Based Implementation Approaches ○ Pre-diffused (or Mask-Programmable) Arrays. ○ Pre-wired Arrays	Rabaey: Ch 8: 8.3-8.5	**LAB03: Programmable Logic Array (PLA) Design and Implementation.**
<u>Module Level (Learning Outcome 2)</u>			
4	**<u>Arithmetic Operations (I) (Arithmetic blocks)</u>** • Datapaths in Digital Processor Architectures • The Adder ○ The Binary Adder: Definitions ○ The Full Adder: Circuit Design Considerations ○ The Binary Adder: Logic Design Considerations	Rabaey: Ch 11: 11.1-11.4	**LAB04: Full Custom Design - "DINO-CMOS" Logic Family**

	• The Multiplier ○ The Multiplier: Definitions ○ Partial-Product Generation ○ Partial Product Accumulation ○ Final Addition		
5	**<u>Arithmetic Operations (II)</u>** • The Shifter ○ Barrel Shifter ○ Logarithmic Shifter ○ Other Arithmetic Operators • Power and Speed Trade-off's in Datapath Structures ○ Design Time Power-Reduction Techniques ○ Run-Time Power Management ○ Reducing the Power in Standby (or Sleep) Mode	Rabaey: Ch 11: 11.5-11.7	**LAB05: Arithmetic Operations**
6	**<u>Designing memory and array structures (I)</u>** • Introduction ○ Memory Classification ○ Memory Architectures and Building Blocks • The Memory Core ○ Read-Only Memories ○ Nonvolatile Read-Write Memories	Rabaey: Ch 12: 12.1-12.3	**LAB05: Arithmetic Operations**

7	**<u>Designing memory and array structures (II)</u>**
	• The Memory Core
	  ○ Read-Write Memories (RAM)
	  ○ Contents-Addressable or Associative Memory (CAM)
	• Memory Peripheral Circuitry
	  ○ The Address Decoders
	  ○ Sense Amplifiers
	  ○ Voltage References
	  ○ Drivers/Buffers
	  ○ Timing and Control
			LAB06: Advanced Memory Design
			- Implementing a Compact and Efficient 6T SRAM Cell

<u>System Level (Learning Outcome 3)</u>			

8	**<u>Coping with interconnect (I)</u>**
	• Interconnect Parameters — Capacitance, Resistance, and Inductance.
	• Capacitive Parasitics
	  ○ Capacitance and Reliability—Cross Talk
	  ○ Capacitance and Performance in CMOS
	• Resistive Parasitics
	  ○ Resistance and Reliability—Ohmic Voltage Drop
	  ○ Electromigration
	  ○ Resistance and Performance—RC Delay
		Rabaey: Ch 4: 4.3 Ch 9: 9.1-9.3	**LAB06: Advanced Memory Design**
			- Implementing a Compact and Efficient 6T SRAM Cell

9	**<u>Coping with interconnect (II)</u>**
	• inductive parasitic
	  ○ Inductance and Reliability—Voltage Drop
	  ○ Inductance and Performance—Transmission Line Effects
	• Advanced Interconnect Techniques
	  ○ Reduced-Swing Circuits
	Current-Mode Transmission Techniques.
		Rabaey: Ch 9: 9.4, 9.5	**LAB07: Crosstalk and Parasitic Study on Digital Schematics**

10	**<u>Timing issues in digital circuits (I)</u>**
	• Timing Classification of Digital Systems
	  ○ Synchronous Interconnect
	  ○ Mesochronous interconnect
	  ○ Plesiochronous Interconnect
	  ○ Asynchronous Interconnect
	• Synchronous Design — An In-depth Perspective
	  ○ Synchronous Timing Basics
	  ○ Sources of Skew and Jitter
	  ○ Clock-Distribution Techniques
	• Latch-Based Clocking.
	• Repeater insertion.
		Rabaey: Ch 10: 10.1-10.3	**LAB8: Clock Generators using DLL**

11	**<u>Timing issues in digital circuits (II)</u>**
	• Self-Timed Circuit Design
	  ○ Self-Timed Logic - An Asynchronous Technique
	  ○ Completion-Signal Generation
	  ○ Self-Timed Signaling
	  ○ Practical Examples of Self-Timed Logic
	• I/Os
		Rabaey: Ch 10: 10.4, 10.6	**LAB8: Clock Generators using DLL**